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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,123	05/08/2001	Martin Czech	Micronas.6247	4156

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,123	CZECH ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2001 and 08 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure filed 08/08/01 and entered as Paper No. 5.

Claim Objections

1. *Claim 1 is objected to* because of the following informality: "said transistors" on line 7 should be replaced by "said laterally designed bipolar transistors". Appropriate correction is required.

2. *Claim 2 is objected to* because of the following informality: "said base zones" (line 5) should be replaced by "said base zone or said base zones". Appropriate action is required.

3. *Claim 6 is objected to* because of the following informality: "at said collector zones" (line 2) should be replaced by "and said collector zones". Appropriate action is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 1*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery (5,043,782) in view of Wada et al (JP361292351A). With reference to Fig. 7: Avery teaches (cf. "Field of Invention", column 1, lines 6-9) an electrostatic discharge (ESD) protective structure that protects an integrated circuit (cf. "Summary of Invention", first line) connected between a first voltage bus 20 (cf. column 4, line 27) with a first supply voltage (inherent) and a second voltage bus or reference line 22 (cf. column 4, lines 27-28), said electrostatic discharge protective structure comprising:

a plurality of laterally designed bipolar transistors QL (cf. column 6, lines 37-42) each having a first load line connected to the first voltage bus 20 and a second line connected to the second voltage bus 22, wherein said first load lines are electrically parallel and said second load lines are electrically parallel to one another (cf. Fig. 7), each of said (laterally designed bipolar) transistors including a control connection to one of the voltage buses, namely the second voltage bus 22 (cf. Fig. 7).

Avery also teaches a resistor (RS) co-integrated into a semiconductor body preceding the control connection for one of the aforementioned laterally designed bipolar transistors QL (the one on the left in Fig. 7; cf. also column 6, lines 44-46).

Avery does not necessarily teach a single-track resistor to precede every control connection *in order to enable a large input surge voltage to be more uniformly dispersed.*

However, Wada et al teach the application of a one track resistor 2 *for this purpose* in an input discharge protection circuit with parallel MIS transistors, as opposed to laterally designed bipolar transistors as in the case of Avery and Applicants (see Figure 2, Abstract, and Constitution in Wada et al). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Avery at the time it was made so as to include the stipulation that a single-track resistor be included as stipulated in claim 1 of Applicants.

Therefore, claim 1 is unpatentable over Avery in view of Wada et al.

3. ***Claims 2-5*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery and Wada et al as applied to claim 1 above, and further in view of Smith (6,075,271).

With regard to claim 2: As detailed above, claim 1 (on which claim 2 depends) is unpatentable over Avery in view of Wada et al. Avery also teaches the electrostatic discharge protective structure of claim 1 wherein the semiconductor body has

embedded therein at least one emitter zone and at least one collector zone (42 and 44 in Fig. 4, respectively) of first conductivity type, and at least one base zone of second conductivity type (58 in Fig. 4).

Neither Avery nor Wada et al necessarily teach a well-shaped region inserted into said semiconductor body between said zones of the first conductivity types and said base zone or zones so as to extend the path length charge carriers have to travel to the base zone.

However, the use of a deeper doped region or well to significantly increase the path length that avalanche generated charge carriers have to travel as a means to increase the collector-to-emitter voltage in bipolar transistor dynamics is a method well known in the art, as witnessed by Smith, who teaches a deeper doped region or well-shaped region 80 (cf. abstract, lines 12-17, and Fig. 7) acting as a barrier for the avalanche-generated charge carriers involved in bipolar snap-back by blocking said charge carriers laterally, increasing the path length to be traversed by them, whereby a higher percentage of them reach the substrate 65 instead and are thus shunted to ground. Because of the specifically stipulated *motivation* as given above and the field of application, namely: technology to increase the bipolar snapback problem, it would have been obvious to one of ordinary skills in the art to modify the invention as essentially taught by Avery and Wada et al so as to include the further limitation of claim 2.

With regard to claims 3-5: the deeper doped region as taught by Smith is connected to zone 110 of first conductivity type (cf. column 4, lines 30-31 and column 7, lines 10-12) (*claim 3*) which is an electrode or source zone (cf. column 7, lines 8-9),

while the examiner takes official notice that electrode or source zones intrinsically have a higher doping concentration than the other regions within the substrate (*claim 4*). The well-shaped region 80 extends more deeply into the substrate than said zone 110 to which it is attached (cf. Fig. 7).

4. ***Claim 6*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery, Wada et al, and Smith as applied to claim 5 above, and further in view of Li et al (5,623,387). As detailed above, claim 5 (on which claim 6 depends) is unpatentable over Avery and Wada et al as applied to claim 1, in further view of Smith. Neither Avery, nor Wada et al, nor Smith necessarily teach the further limitation of claim 6. However, the lateral enclosure of transistors by doped zones connected through metal contacts is well known in the art as an obvious way (creation of equipotential lines through enclosure by conductors) of creating favorable conditions for a more uniform conduction of current between emitter and collector zones in transistors, as witnessed by Li et al, who teach an esd protection circuit (cf. title) involving a bipolar transistor (cf. abstract), specifically the surrounding of first conductivity type emitter and collector zones 431, 435, by second conductivity type zones 422 connected to a common metal contact 423 (cf. Fig. 6B; see also Fig. 7B) (cf. column 13, lines 54-59). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of claim 5 so as to include the further limitation of claim 6.

5. ***Claims 7- 12*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery, Wada et al, Smith, and Li et al as applied to claim 6 above, and further in view of Wong et al (6,277,689). As detailed above, claim 6 (on which claim 7 depends) is unpatentable over Avery, Wada et al, and Smith, in further view of Li et al.

Avery, Wada et al, Smith, nor Li et al, necessarily teach the further limitation defined by claim 7, except for the presence of charge carriers of the first conductivity type (see Smith, column 1, lines 37-43).

However, the use of embedded wells for the purpose of combating volatility in lateral bipolar transistors is well known in the art as witnessed by Wong who teaches a P-well 34 embedded in an N-well 36 within a substrate 38 (cf. Fig. 4 and column 3, lines 60-64).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 6 at the time at the time of the invention so as to include the further limitation of claim 7.

With regard to claim 8: emitter and collector zones 42 and 44, respectively, as shown in Fig. 4 of Avery are designed as strips and are disposed alternatingly next to one another and parallel to one another. Thus the further limitation of claim 8 does not distinguish over the prior art.

With regard to claim 9: Figure 6 in Avery shows that the electrostatic discharge structure of Avery configured and arranged in an essentially square layout. Thus the further limitation of claim 9 does not distinguish over the prior art.

With regard to claim 10: the examiner takes official notice that the provision of thorough contacts between electrodes and emitter/collector regions is an obvious requirement for any transistor: without it the current through the device would be impeded and the voltage between emitter and collector would be compromised. Therefore, the further limitation of claim 10 does not distinguish over the prior art.

With regard to claim 11: The electrostatic discharge structure taught by Wada et al comprises emitter and collector electrodes connected via conductor tracks (inherent property of electrodes in any working electronics device of which they form a part) to oppositely situated voltage buses (cf. Fig. 2) and form finger-like connections (four fingers on each side in Fig. 2) which are staggered with one another so as to render as much electrostatic balance to the configuration as possible, as indicated by the locations L1, L2, L3, and L4 in Fig. 1 in Wada et al.

With regard to claim 12: the bipolar transistor electrostatic discharge structure as taught by Avery is designed as a field oxide bipolar transistor structure, as shown by Fig. 5.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nathan Flynn
Primary Examiner

JPM
February 7, 2002